IN THE DRAWINGS

The label in Figure 1 has been amended from "FIGURE 1" to "FIGURE 1 (Prior Art)". No new matter has been added as result of the amendment to the Drawings. A Submission Of Drawings is being filed herewith.

REMARKS

Claims 1-23 remain pending in this application. Claims 24-26 were newly added. Claims 1, 8, 12, 13 and 17 were amended. Therefore, claims 1-26 are pending in the present application.

The label in Figure 1 has been amended from "FIGURE 1" to "FIGURE 1 (Prior Art)". No new matter has been added as result of the amendment to the Drawings. A Submission Of Drawings is being filed herewith.

The Examiner rejected claims 1-7, 12, and 17-23 under 35 U.S.C. § 112, second paragraph. The claims rejected under 35 U.S.C. § 112, second paragraph have been amended to address the Examiner's concern. Regarding the issue of "a virtual memory address" being indefinite (see Paragraph 6, Item B (ii) of page 3 of the Office Action Dated March 15, 2005), Applicants respectfully assert that this term is not definite since it is well known by those skilled in the art. Furthermore, this term is provided in the Specification (*see* for example, last paragraph of page 11 of the Specification). In light of the amendments and arguments provided herein, Applicants respectfully assert that the rejections under 35 U.S.C. § 112, second paragraph, are now moot and request that the Examiner withdraw these rejections. Therefore, claims 1-7, 12, and 17-23 are allowable.

In the Office Action, claims 1-23 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of co-pending U.S. Patent Application Serial No. 09/999,881 filed on October 31, 2001. Although Applicants believe that the claims of the present invention call for an invention that is different from the

claims of U.S. Patent Application Serial No. 09/999,881, in the interest of expediency, Applicants have included herein a Terminal Disclaimer and respectfully request that the Examiner's provisional rejection of claims 1-23 be withdrawn. However, it will be appreciated that the filing of the Terminal Disclaimer to obviate the Examiner's rejection is not an admission of the propriety of the rejection. *Quad Environmental Technologies Corp. vs. Union Sanitary District,* 946 F.2d 870, 20 USPQ2d 1392 (Fed Cir. 1991). See, *e.g.*, MPEP §804.03.

The Examiner rejected claims 1-4, 6-20, 22, and 23 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,745,307 (***McKee***). Applicants respectfully traverse this rejection.

Applicants respectfully assert that ***McKee*** does not teach, disclose or suggest all of the elements of claim 1 (as amended) of the present invention. For example, the virtual memory access called for by claim 1 of the present invention calls for performing a virtual address based memory access that is based on a secondary table and at least one virtual memory table. The Examiner asserted that this element is anticipated by the usage of the TLB and the virtual page address 505 of ***McKee.*** The Examiner asserted that this disclosure anticipated the use of the secondary and of virtual memory table of claim 4, as well as claim 1 (as amended). Applicants respectfully disagree. Applicants respectfully assert that the use of the secondary table as well as the virtual memory table is not anticipated by the TLB and the virtual page address 505 of ***McKee***.

The TLB is a translation look-aside buffer. The TLB contains data that is actually written by an operating system. For example, ***McKee*** discloses that the virtual page table entry 602 contains additional fields from which information required for a TLB entry can be retrieved. See

col. 8, line 66 col. 9, line 1. ***McKee*** discloses that if the operating system successfully translates the virtual memory address into a physical memory address, that translation, both as a virtual page table entry and as a TLB entry, is inserted into the TLB. See col. 9, lines 1-4. This disclosure makes it clear that data is entered into the TLB as a result of translating virtual memory address into physical memory address, and not used to perform a virtual address based memory access. In other words, the virtual address based memory access is not performed using the TLB and the virtual page table 602, contrary to the Examiner's assertions. In fact, the above cited passage in ***McKee*** makes it abundantly clear that the prior art discloses that memory access is performed prior to writing data into the TLB *i.e.*, the virtual memory address being translated into a physical memory address. Subsequently, that information is then entered into the TLB. Therefore, it is erroneous to argue that the virtual address memory access in ***McKee*** is performed using two entities, such as the TLB and the virtual address table. Hence, the disclosure of the memory access in ***McKee*** is in stark contrast with the virtual address based memory access called for by claim 1 of the present invention, which calls for using a secondary table and a virtual memory table. Therefore, Applicants respectfully assert that the usage by ***McKee*** of the TLB and the virtual page table do not equate, anticipate or make obvious the element of the virtual address memory based access called for by claim 1, which calls for using a secondary table and a virtual table access.

In fact, ***McKee*** simply does not disclose a secondary table. The Examiner's usage of the TLB is erroneous since data is written into the TLB, wherein virtual memory access called for by claim 1 of present invention uses information in the secondary table as well as a virtual memory table. In other words, ***McKee*** does not anticipate the subject matter of virtual address memory

access using a secondary table and a virtual table access. Therefore, claim 1 of the present invention is not taught, disclosed or suggested by ***McKee***. Accordingly, claim 1 of the present invention is allowable.

Similarly, claim 8 calls for a method that provides for the memory access using a virtual address, wherein the access includes utilizing a secondary table, as well as at least one virtual memory table. Additionally, claims 12, 13 and 17 call for various apparatus and/or computer systems that called for performing a memory access using a virtual address, wherein the access includes utilizing a secondary table as well as at least one virtual memory table. Therefore, claims 8, 12, 13 and 17 are also not taught disclosures suggested by ***McKee*** for at least the reasons cited above.

Independent claims 1, 8, 12, 13, and 17 (all as amended) are allowable for at least the reasons cited above. Additionally, dependent claims 2-7, 9-11, 14-16, and 18-23, which respectively depend from claims 1, 8, 12, 13, and 17, are also allowable for at least the reasons cited above.

Applicants acknowledge and appreciate that the Examiner asserted that claims 5 and 21 contained allowable subject matter. Additionally, newly added claim 24 comprises subject matter that the Examiner has asserted is allowable and, therefore, is also allowable for at least the reasons cited herein.

Reconsideration of the present application is respectfully requested. In light of the arguments presented above, Applicants respectfully assert that claims 1-26 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, **the Examiner is requested to call the undersigned attorney at the Houston, Texas telephone number (713) 934-4069** to discuss the steps necessary for placing the application in condition for allowance.

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Respectfully submitted,

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